ARC-46: 8-Channel IR Video Processor

This document describes the eight channel IR video processor, part number ARC-46, Rev. 3A. In each of its eight identical video processors there is a balanced differential input stage, an offset nulling and gain stage, a resettable integrator and a 18-bit, 0.5 microsecond conversion time A/D. Image data is transferred to the controller backplane through a FIFO circuit, and DC bias supplies provide seven programmable voltage output for controlling IR arrays. It operates with the 250 Mhz fiber optic timing board in a compact and cost effective system that is targeted to operate 32-channel and even 64-channel IR arrays. The current revision 3A, first available in the summer of 2007, differs from earlier revisions primarily in having better A/D converters and a different input connector.

Video Processing

The input stage of each video channel has space for the user to install through-the-hole passive components. Referring to channel A, the source load resistors R10 or R21 may be installed by the user. The SOURCE line connects the source load resistor either to ground (JP11 pins 2-3) or to the DC bias voltage (JP11 pins 1-2) BIAS7 whose voltage is programmable. The resistors 249 ohm R5 and R26 are installed to connect the array signal to the input buffer. The capacitors C7 and C20 may be installed by the user to act as low pass filters in conjunction with R10 and R21 for bandwidth control, although these were not installed for the performance tests described later in this document.

After these input networks there are identical unity gain, low noise buffer stages on each of the inverting and non-inverting input networks, providing a fully balanced, high impedance input stage. The outputs of each buffer stage are brought to an op amp configured as a differential amplifier with unity gain. After this differential stage the video signal is fed into the inverting input of an AD829 op amp configured with a gain of x5. A DC offset nulling level is fed into the non-inverting input of this gain stage, providing for nulling of the IR array over a range of -3 to +5 volts.

Following this is an integrator stage whose gain is proportional to the integration time and inversely proportional to the product of its input resistance and feedback capacitance. The feedback capacitance is fixed at 1nF, while the input resistance has two software selectable values, 4k for low gain, slow readouts or 1k for high gain, fast readout. Note that the shortest pixel time is 2.6us/pix for a 32 channel detector, which is limited by the fiber optic speed of 12.5 Mpixels/sec.

All resistors which directly influence the video gain have a tolerance of 0.1% and a temperature coefficient of 10 parts per million (ppm). All other resistors are 1% and temperature coefficients of 50 to 100ppm. The capacitor in the integrator has a

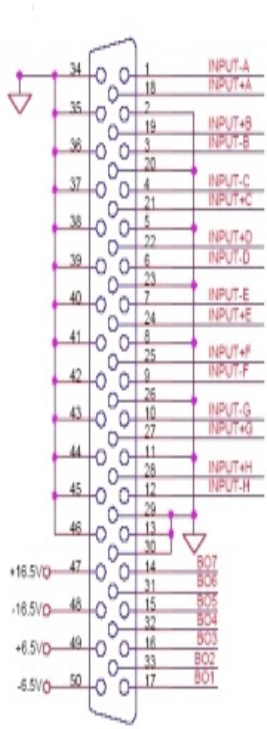
temperature coefficient with a range of 0 to 50 ppm, with a mean of 25 ppm. It will dominate the circuit's gain variability with temperature.

The software delivered with the controller is written to process the following approximate input voltage range, typical of HAWAII arrays:

Input voltage = 0.55 volts	A/D counts = 0 = dark level
Input voltage = 0.0 volts	A/D counts = 64k = full well

The A/D converters are configured with an input voltage range of -2.5 to +2.5 volts, so this is about a factor of 10 overall analog gain. The input amplifier stage provides a gain of 5, while the integration time of nearly 2 microsec with the integrator RC values of 1k and 1nf provide an integrator gain of close to 2, for an overall gain of about x10. To operate in this mode the pins on the DB-50 male connector are connected so that the + input goes to the detector and the - input goes to ground or a reference voltage less than the detectors' output source voltage. The input connector is a triple row, 50-pin DB male connector, Positronic part #MD50M5R400X. We generally supply the matching female connector #MD50F20000. The pinout for the connector is shown in the tables below, along with a schematic representation of the connector. The pinout of the connector is as follows:

Pin #	Function	Pin #	Function
1	Input -A	18	Input +A
3	Input -B	19	Input +B
4	Input -C	21	Input +C
6	Input –D	22	Input +D
7	Input -E	24	Input +E
9	Input –F	25	Input +F
10	Input -G	27	Input +G
12	Input –H	28	Input +H



Four bits are used in the pixel routine to trigger switches in the video chain.

Bit 3	SS3	Move A/D value to the FIFO on high going edge
Bit 2	SS2	Start A/D conversion on low going edge
Bit 1	SS1	Reset Integrator when low
Bit 0	SS0	Integrate when low

A typical video processing timing is as follows:

1. Integrate	%0110
2. Wait for setting time	%0111

3.	Start A/D conversion	%0011
4.	Hold A/D input for at least 400ns	%0111
5.	Clock the next pixel's charge	
6.	Move A/D data to the FIFO	%1111
7.	Reset Integrator	%0101
8.	Wait for settling time	%0111
9.	Transmit data to host	(SXMIT)
10.	Wait for settling time	%0111

As shown in step 1, SS0 is cleared to begin integration. This causes the PAL to set either the switch line INTEGRATE 1* or INTEGRATE 2*. If INTEGRATE 1* is set then the 4K input resistor is switched through to the integrator circuit (slow readout), and if INTEGRATE 2* is set then the 1K input resistor is switched through to the integrator circuit (fast readout). Which line is switched through depends on the value previously written to the PAL during the DAC set up procedure. (0xnC3xx0 for INTEGRATE 2*, and 0xnC3xx1 for INTEGRATE 1*). This operation is done for each video board "n" in the system, and is located in the *.waveforms file -

0xnC3001	Slow, low gain integration, 4k resistor, n = board number
0xnC3000	Fast, high gain integration, 1k resistor, n = board number

There are two FIFOs that buffer the image data between the A/D converters and the backplane. The FIFOs on all the boards in the system can be reset with a single global command -

0x0C1000	reset all image data FIFOs in the controller

This can be done outside the initialization process using a command -

```
MOVE    #$0C1000,A      ; Clear image data FIFO
JSR     <XMIT_A_WORD
```

The following stages convert the single ended output of the integrator to differential signals required by the Analog Devices AD7641 A/D converter. It is a fast 18-bit part that samples its input during the time before its start A/D signal goes high to initiate the conversion. The digital output data from each of the eight A/D converters are written to a single FIFO, and then transmitted to the backplane through one of two latches. One latch maps the most significant of the 18 A/D bits to the 16 backplane lines for transmission by the timing board to the computer, whereas the other latch maps the least significant 16 bits. Selection of which of these modes is operational is made in software as described below.

Digital Interface

The DAC and switch address of the video board are selected via a jumper block located next to the big PAL near the backplane connector. However, unlike the clock board the address/switch jumper logic is such that an installed jumper corresponds to a one, and an uninstalled jumper to a zero. The four jumpers marked "A/D DAC" must be uniquely set on each board in a system so each can be individually addressed, while the four jumpers marked SWITCH are generally set to the same values so the timing for all boards in a system is identical. The synchronous serial interface(SSI) lines STD and SCK of the timing board DSP56303 are used to write to the DACs on the board, where a 24-bit serial word is sent and the most significant four bits are compared to the "A/D DAC" jumper settings. The signals for reading the A/D image values are TIM-ADSTR and TIM-ADA# discussed above, and are compared to the jumper settings "A/D DAC" on each video board. Pixel timing is written by the timing board DSP to is address WRSS and transferred over the backplane over the 12 timing lines SS0 to SS11 and its strobe signal WRSS, while the lines SS12-16 are compared to the jumpers "SWITCH".

The transmission of data to the host is generated by the SXMIT word executed by the timing board, which is of the format $00Fxxx. The least significant 12 bits determine which channels are to be transmitted to the host. The least significant six bits determine the start channel number and the next six bits determine the end channel number. For example,

SXMIT	Least Significant 12bits	Channel Start	Channel End
$00F1C0	%*0001 11***00 0000**	**0**	7
$00F3C0	%*0011 11***00 0000**	**0**	15
$00F7C0	%*0111 11***00 0000**	**0**	31
$00F7CF	%*0111 11***00 1111**	**15**	31
$00F246	%*0010 01***00 0110**	**6**	9
$00F000	%*0000 00***00 0000**	Channel ***0*** only	
$00F041	%*0000 01***00 0001**	Channel ***1*** only	
$00F1C7	%*0001 11***00 0111**	Channel ***7*** only	

The SXMIT value is used by the timing board to calculate how many channels are to be transmitted and from which video boards. The timing board strobes the line TIM_ADSTR the required number of times, writing the seven bit A/D addresses TIM_ADA0 to TIM_ADA6. The most significant line TIM_ADA6 is always low, but has been wired in for future expansion to a larger number of channels.

For example, if channels 6 to 9 were to be transmitted then SXMIT would have the value $00F246, and the timing board would generate four strobes on TIM_ADSTR, writing the

following values to TIM_ADAD# on each strobe:

%0000110	(video board 0)
%0000111	(video board 0)
%0001000	(video board 1)
%0001001	(video board 1)

The four jumpers marked "DAC A/D" set the address that the board will respond to when writing to the DC bias DAC or reading image data. These must be set to different values for each video board in a system so each board can be uniquely addressed, whereas the “SWITCH” jumpers are usually set to the same value for all video boards in the system so they all operate with the same timing. There are two modes for transferring image data from the A/Ds to the image data FIFO. In the “eight-channels-all-at-once” mode (TIM_V_AUX1 = 0) all eight A/D values on each board are transferred in turn to the image data FIFO on the rising edge of XFER. They will be transmitted over the backplane whenever the bits TIM-ADAD:6-3 match the jumpers "DAC A/D" on each video board starting with A/D#0 and ending with A/D#7, ignoring the bits TIM-A-ADAD:2-0. In the 'one A/D at a time mode' (TIM_V_AUX1 = 1) the addresses TIM_ADAD:2-0 select which of the eight A/Ds on the board gets its data written to the FIFO, after which it is written directly to the backplane and transmitted to the host computer. The default software supplied with the system has the “one-at-a-time” mode selected.

There are two advanced provisions for extending the capabilities of the board somewhat. The AD converter has a special mode called WARP that allows it to run at a higher speed than the normal mode, but with a restriction on the length of time allowed between conversions. Also, the 18-bit A/D converters can have either their least or most significant 16 bits transmitted to the host computer. The default is to transmit the most significant bits, and selecting the least significant bits may be useful for careful noise analysis.

High 16 bits selected (default)	0xnC2000
Low 16 bits selected	0xnC2001
WARP off (default)	0xnC2002
WARP on	0xnC2003

"n" is the board number, from 0 to 15. These can be included in the waveforms file or written with the XMIT_A_WORD subroutine.

DC Bias Supplies

There are seven external DC bias lines available from the video board. Three of these biases are fixed bipolar (±5V) and the other four are selectable as either unipolar positive, unipolar negative or bipolar. Their polarity is set by the jumpers JP9 and JP10. A jumper placed closest to the edge of the board in JP10 will set the lower voltage to zero volts, and in placed furthesst from the edge will set it to -5 volts. A jumper placed in JP9 nearest the board edge will set the upper voltage to zero volts, and furthest from the edge to +5 volts. Furthermore, the video board has ±16.5V and ±6.5V levels available from a Dtype connector. Note that these values can be adjusted using pot trims in the large power supply. These are available on the male DB-15 front-panel connector P2, with the pinout below. n is the board number and xxx is the 12-bit value written to the DAC to set the output voltage:

Pin #	Voltage range	Address
17	-5 to +5 volts	0xnc4xxx
33	-5 to +5 volts	0xnc8xxx
16	-5 to +5 volts	0xnccxxx
32	-5 to 0, 0 to +5 or -5 to +5 volts	0xnd0xxx
15	-5 to 0, 0 to +5 or -5 to +5 volts	0xnd4xxx
31	-5 to 0, 0 to +5 or -5 to +5 volts	0xnd8xxx
14	-5 to 0, 0 to +5 or -5 to +5 volts	0xndcxxx
47	+16.5 volts from the power supply	
48	-16.5 volts from the power supply	
49	+6.5 volts from the power supply	
50	-6.5 volts from the power supply	

The +/- 5 volt range of these circuits can be changed by the user by installing a different resistor in the reference voltage generating circuitry near the reference U86. The resistor R286 is installed as a value of 1k, and is employed in a current summing circuit. Larger values may be installed to reduce the voltage range, which is advisable if the board is used to generated DC bias voltages for the new generation of Rockwell H1RG and H2RG parts that are designed with 3.3 volts rules. Also provided for protection is provision for installing zener diodes to limit the excursion of the DC bias supplies. They can be installed in the header D1 located near the front panel.

There are also eight DC offset null biases available, one for each channel. These can be selected between -3V and 5V. There is filtering on offset nulls via a 470uF capacitor and 1kΩ resistor, resulting in a 0.5s time constant. This is used to beat down 1/f noise and reduce drift. If an array read is taken soon after a power on, then a gradient across the readout will be visible as this capacitor charges.

All biases are established using the standard 12bit DACS (with a temperature coefficient

of 4ppm) used in other controller boards. There are 16 bias levels in total: 8 video-offset nulls, 7 external biases, and one gain select level for the ADC. Nominally this ADC utilizes ±2.5V references, however, this can be reduced with the DAC bias level to increase the gain. This allows an increase in gain without influencing bandwidth (unlike the integrator whose gain increases with integration time while its bandwidth decreases). Consequently, there are three ways to alter the gain of the video chain: (1) by switching the integrator resistor, (2) by changing the integrator time, and (3) altering the ADC reference voltage.

The board addresses for each of these DACs is listed below, and used in the waveform file "ARC46.waveforms":

Function	Address	Function	Address
Offset ChA	0xne0xxx	Offset ChE	0xnf0xxx
Offset ChB	0xne4xxx	Offset ChF	0xnf4xxx
Offset ChC	0xne8xxx	Offset ChG	0xnf8xxx
Offset ChD	0xnecxxx	Offset ChH	0xnfcxxx
A/D reference	0xnc0xxx		

Data Transfer Rate

A PCI bus analyzer was used to investigate the data transfer across the PCI bus to evaluate the efficiency of various processes. In Version 1.8 of the PCI code, data is written across the bus in 16 pixel bursts (8 x 32 bit writes). Here the duty cycle of the burst is approximately 50%. That is, the times to set up and to actually perform a burst write are approximately equal. With this burst length the maximum data rate was about 9 Mpixels/sec, below the maximum fiber optic data rate of 12.5 Mpixels/sec, and indeed images could not be transferred successfully at that rate. The burst length was increased from 16 to 128 pixels by adjusting the parameters in the "pciboot.asm" file marked with an "(!!!)" in the comment field. With this adjustment the duty cycle improved to 76%.

It should be noted that even in burst mode the transfer of data is not 100% efficient, i.e. not continuous. The PCI bus maximum data transfer rate is 133.3Mbytes/s, so a 32bit write takes 30ns. However, the 64 pixel burst write (32 x 32bit writes) transfer time was measured as 1860ns, which averages to 58ns per 32 bit write. This is because there are occasional transfer set up times, which vary from word to word (usually 0 or 30ns and sometimes 60ns). This time in conjunction with the PCI and DSP overheads results in a total bus bandwidth usage of over 50% for the sustained data rate of 12.1Mpixels/sec.

Note that 12.5Mpixels/s (25Mbytes/s) sustained transfers will utilize 18.8% of the bus bandwidth if the transfer of data were 100% efficient. With the loss of efficiency due to DSP overheads the PCI bus utilization was measured to be 39% at the maximum fiber optic transfer rate of 12.5 Mpix/sec, and fully reliable.