## **Waveform Generator**

Application Note 03 Monday, July 19, 2021

The ARC-420 timing board FPGA contains a waveform generator that controls 16 signal lines on the controller's backplane that are received and interpreted by the ARC-430 clock driver and ARC-440 video boards to control their timing. These 16 signal lines, named SS15 to SS0 for signal state, are controlled by a waveform table and associated circuitry resident in the FPGA that is in turn controlled by commands sent from the micro-controller. Each micro-controller command instructs the FPGA to write a sequence of 16-bit data words from the waveform table to pins that are routed to the backplane pins SS15-SS0. This sequence is generated from one of a large number of waveform arrays in the waveform table, each array containing 32-bit words that are read in order by the waveform generator. The first entry in each waveform array is the length of the waveform array and is followed by the waveform array values. Each value consists of a 16-bit delay number and a 16-bit data value that controls SS15-SS0. After the 16-bit data field is written to SS15-SS0, the waveform generator waits by the delay number times 20 ns before processing the next value. Once the waveform generator reaches the end of the waveform array it decrements a loop counter and loops back to the beginning of the array if it is non-zero.

The construction of the FPGA waveform generator table is from an ordered list of waveform definitions, which are defined in the micro-controller source code, and written to the FPGA memory during controller initialization. The order in which waveform definitions are written into the waveform table is determined by the micro-controller code waveform list definition. The stored order of a waveform has no bearing on its execution. The micro-controller source code on the following pages shows the waveform array named FRAME\_INIT being loaded into the FPGA waveform generator table and then executed using the Arc420\_WGWriteCommand.



The following micro-controller call will cause the FPGA to execute the FRAME\_INIT\_WAVEFORM one time:

Arc420\_WGWriteCommand( FRAME\_INIT\_WAVEFORM.addr, 1 ); waveform start address which is 0 for loop count FRAME\_INIT\_WAVEFORM To view the waveform table in G4, click the button on the waveform generator section in the setup window:



Then click the Run button on the window that appears:

ଞ୍ଯ WG Curr	ent Table Values			- 0	×
				Γ	Run
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Current	WG Table Val	ues			
0×000	0×00000003	0x00311003	0x00311002	0x00001003	
0x004	0x00000003	0x00311003	0x00311005	0x00311003	
0×008	0x00000004	0×0031100B	0x00311003	0×0031100B	
0×00C	0x00C71003	0×00000004	0x0004100B	0x00040003	
0×010	0x00040000	0x00041003	0x00000003	0×0009100B	
0x014	0x0019417C	0x00311003	0x00000003	0x00311003	
0x018	0x00311007	0x00311003	0x00000004	0x00188000	
0x01C	0x00189F0F	0×00181020	0x00189F30	0x00000005	
0x020	0x00189F0F	0×00181010	0x00189F30	0x00180000	
0x024	0x00188002	0×00000001	0x0000C80F	0x00000001	
0x028	0x0000C000	0x0000003	0x00189000	0x00311FFF	
0x02C	0x00181000	0x0000003	0x00181003	0x00181002	
0x030	0x00001003	0x0000003	0x00181003	0x00181005	
0x034	0x00181003	0x0000003	0x00181003	0x00181005	
0x038	0x00181003	0x00000004	0×0018100B	0×00181003	
0x03C	0×0018100B	0×00181003	0x00000005	0x00041003	
0x040	0x00020003	0×0000100B	0x00010000	0×0004100B	
0x044	0x00000003	0x00181003	0x00181007	0x00181003	
0x048	0x00000005	0x0031903F	0x00311300	0x00311200	
0x04C	0x00311300	0x00319F30	0x00000002	0x0009913F	
0x050	0x00091000	0x00000002	0x00091800	0×00091C00	
0x054	0x00000002	0x00091000	0x00091400	0x00000002	
0x058	0x0009913A	0×00091000	0×00000002	0x00091003	
0×05C	0x00091007	0x00000002	0×00091002	0×00091006	
0×060	0x00000002	0×00091200	0x00099F30	0x00000000	-